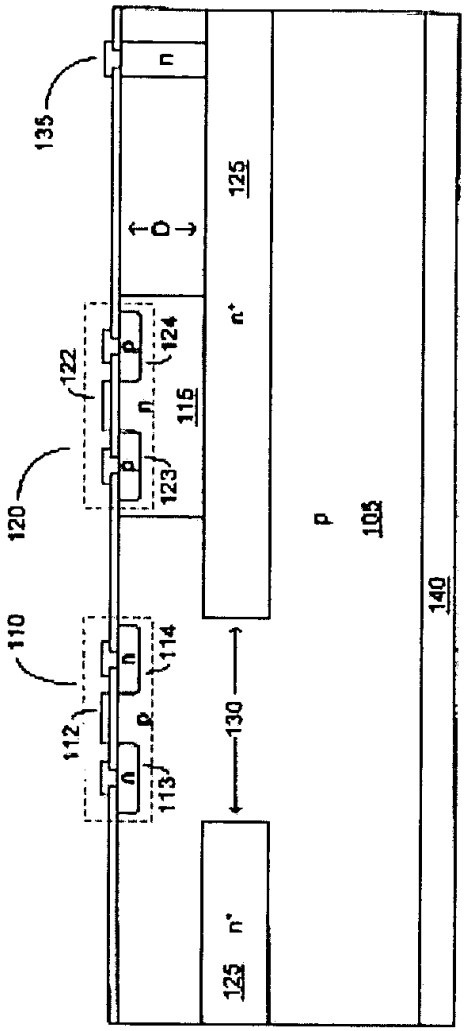

Figure 1
(Prior Art)

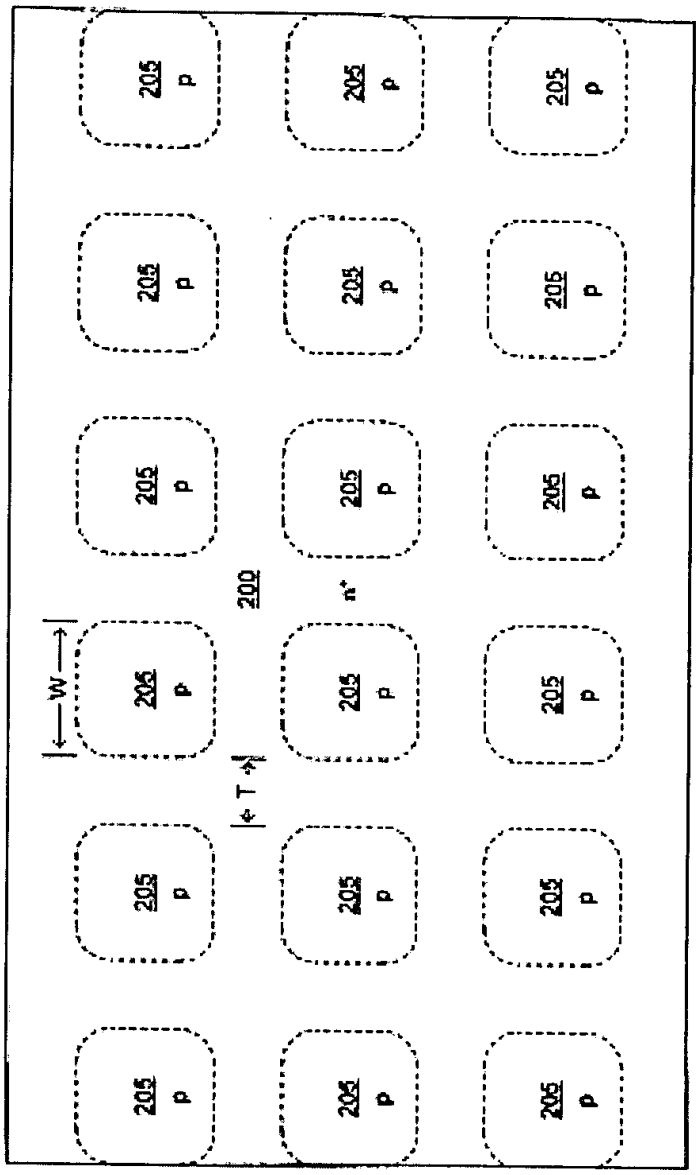

Figure 2A

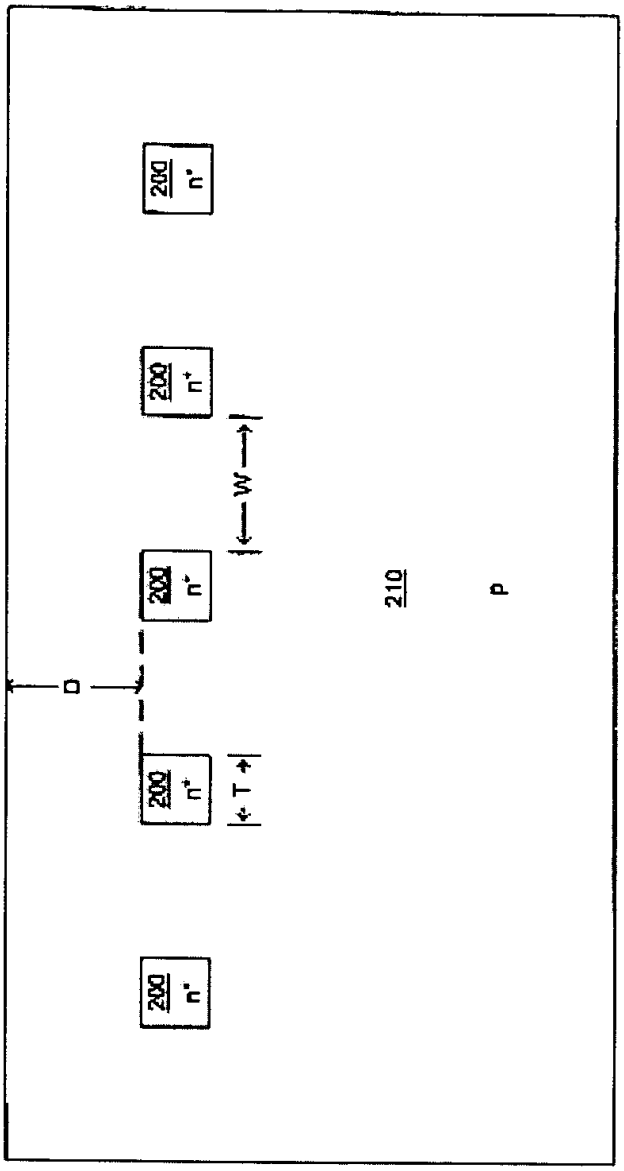

Figure 2B

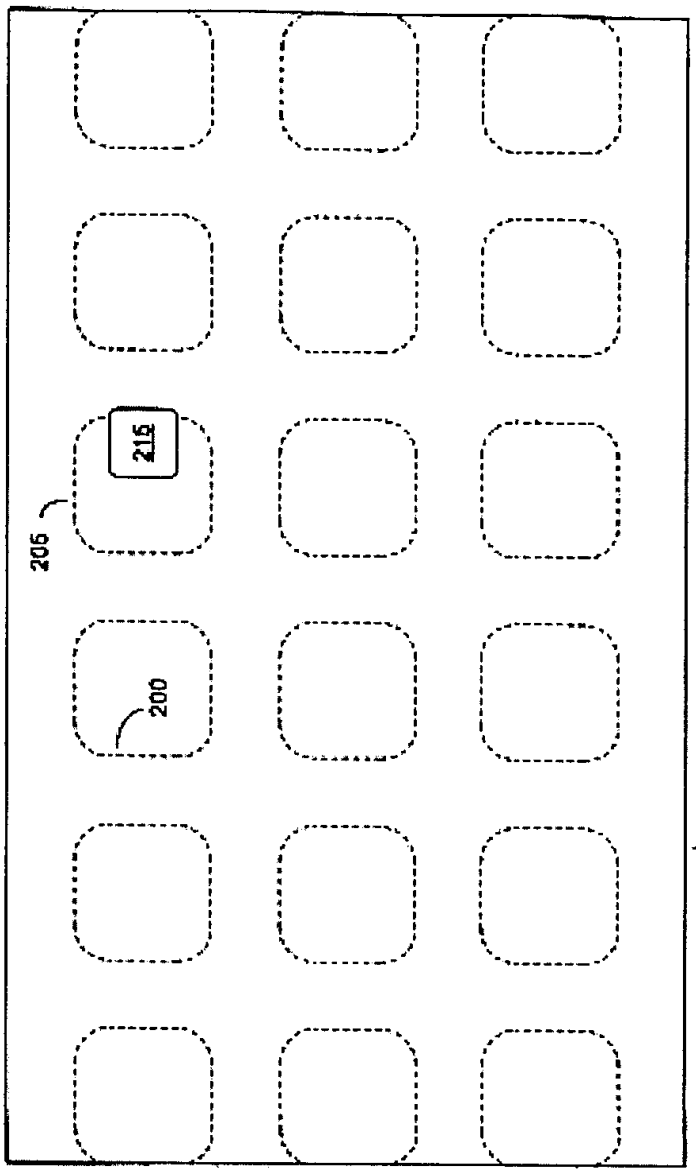

Figure 3A

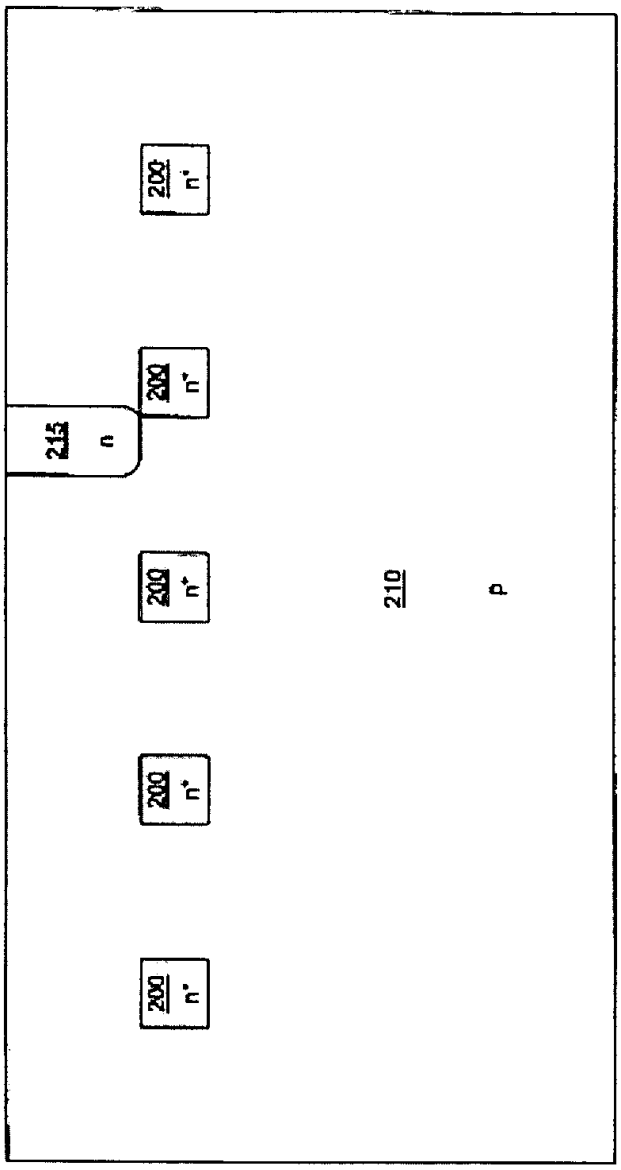

Figure 3B

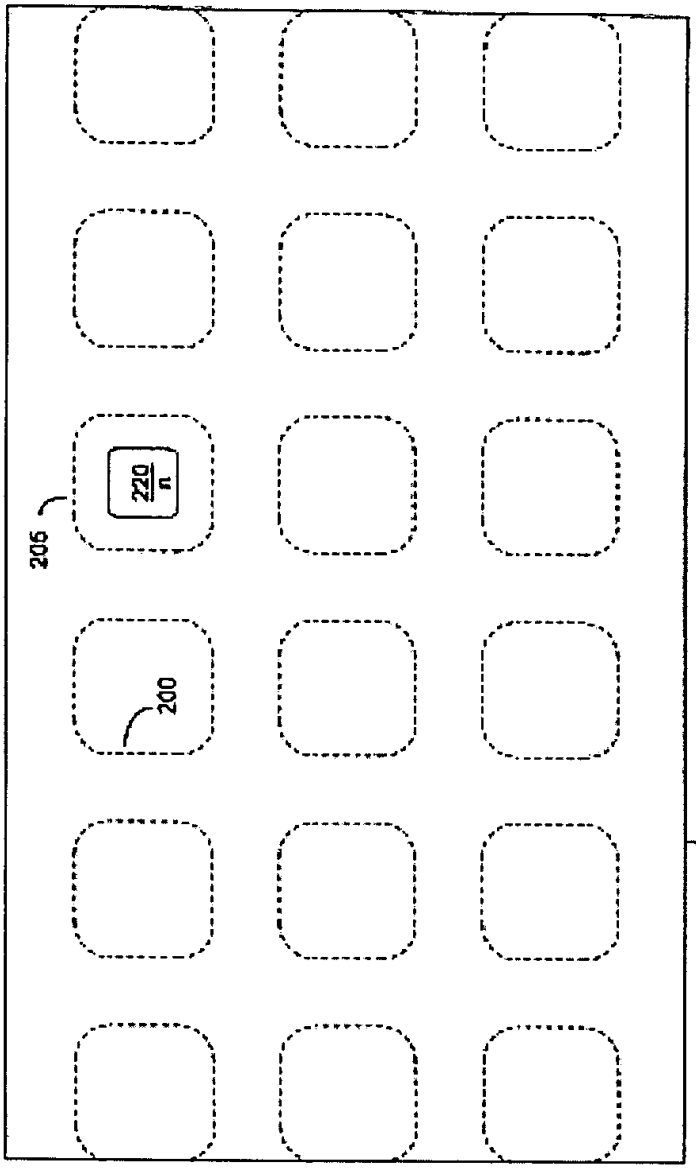

Figure 4A

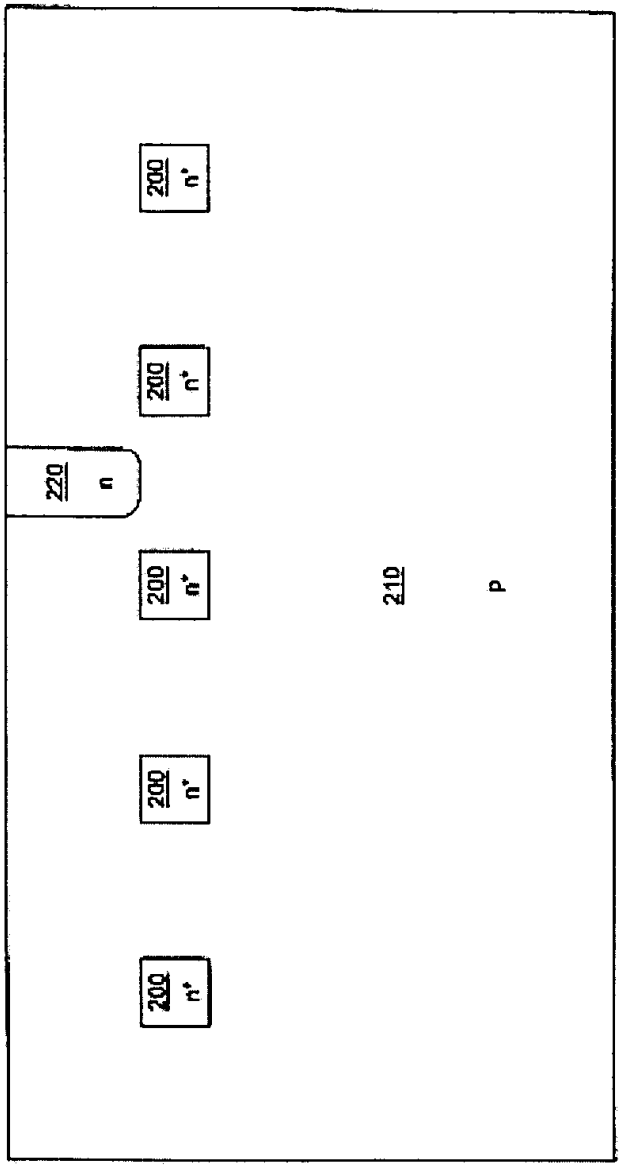

Figure 4B

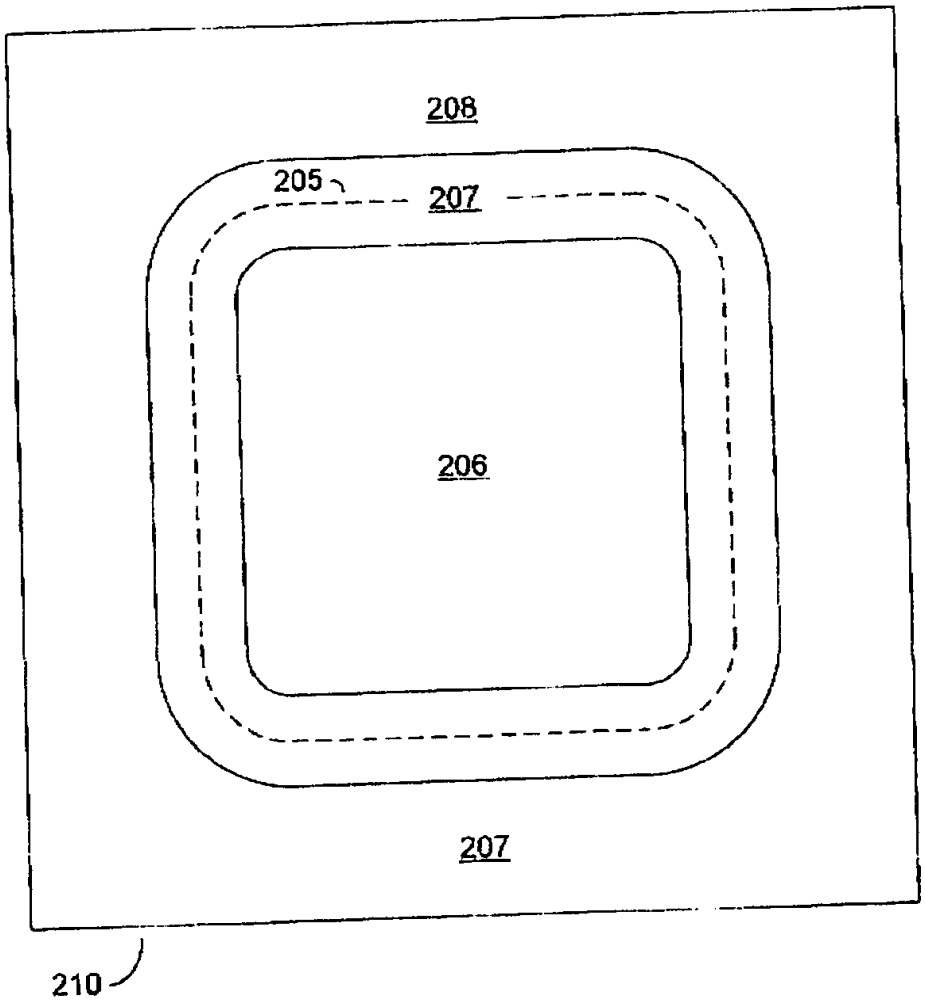

Figure 4C

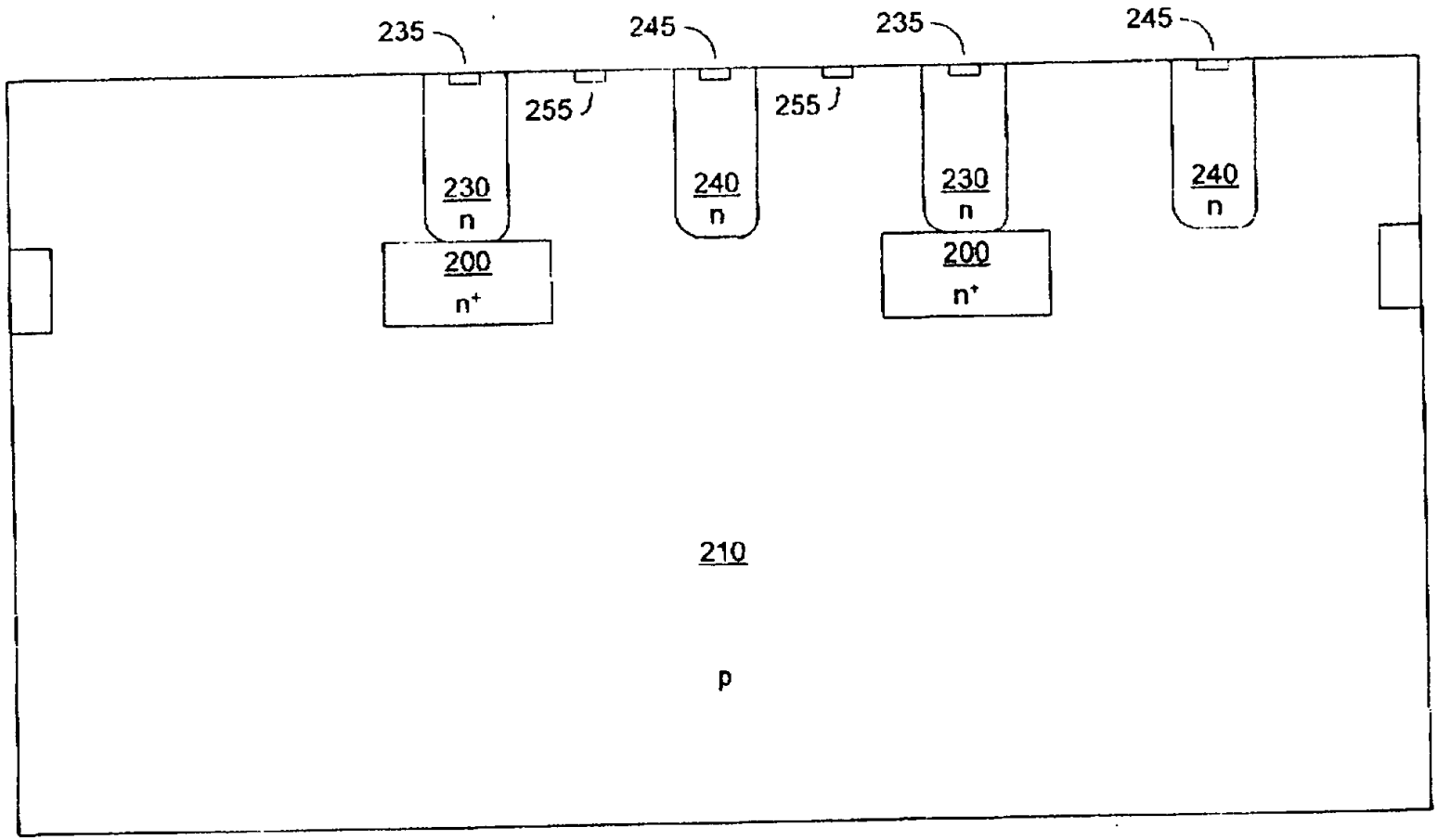

Figure 4D

500

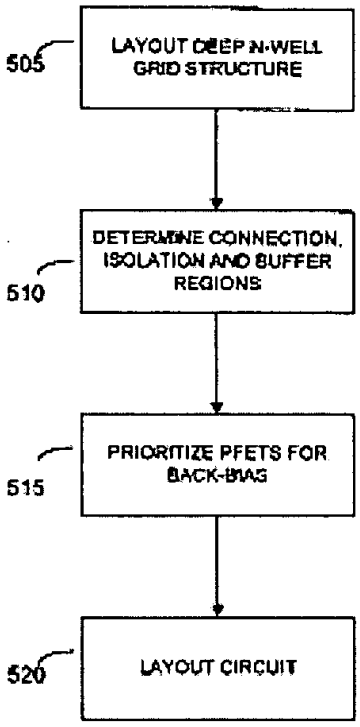
505
LAYOUT DEEP N-WELL GRID STRUCTURE
510
DETERMINE CONNECTION, ISOLATION AND BUFFER REGIONS
515
PRIORITIZE PFETS FOR BACK-BIAS
520
LAYOUT CIRCUIT

Figure 5

600

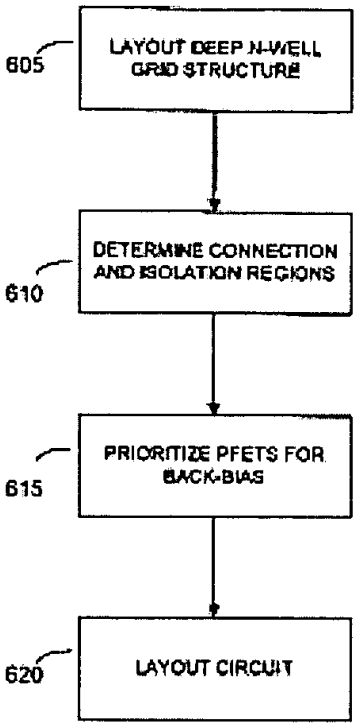
605
LAYOUT DEEP N-WELL GRID STRUCTURE
610
DETERMINE CONNECTION AND ISOLATION REGIONS
615
PRIORITIZE PFETS FOR BACK-BIAS
620
LAYOUT CIRCUIT

Figure 6

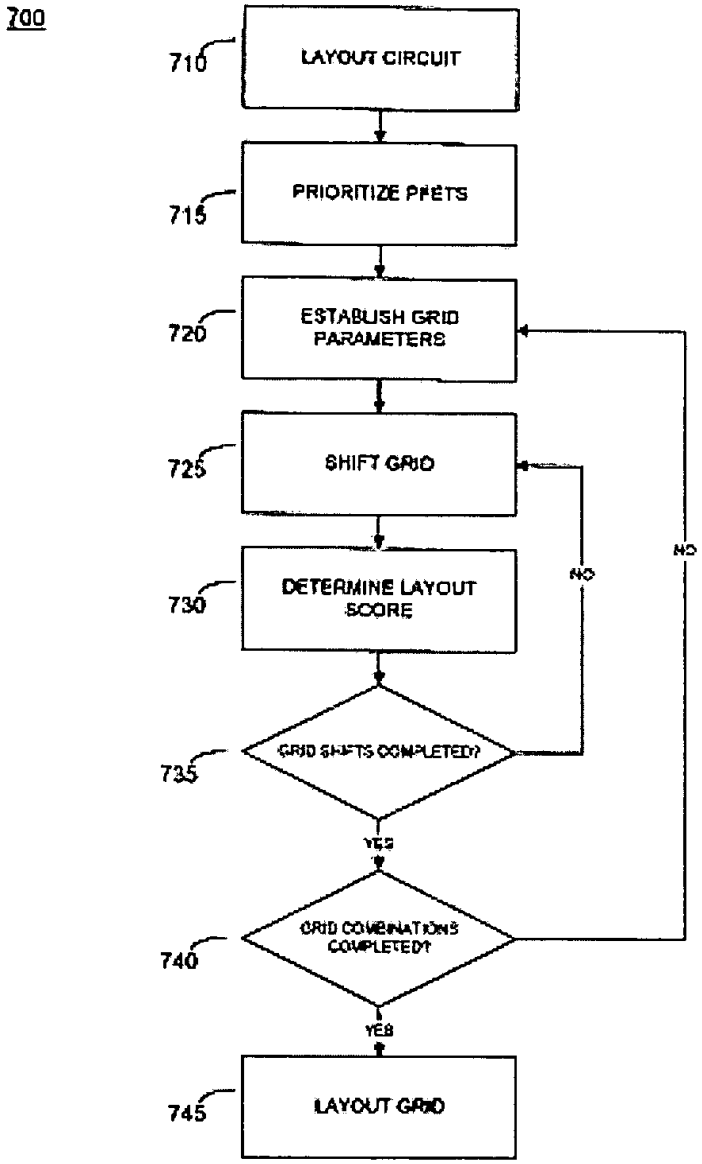
700
710
LAYOUT CIRCUIT
715
PRIORITIZE PNETS
720
ESTABLISH GRID PARAMETERS
725
SHIFT GRID
730
DETERMINE LAYOUT SCORE
735
GRID SHIFTS COMPLETED?
NO
YES
740
GRID COMBINATIONS COMPLETED?
NO
YES
745
LAYOUT GRID

Figure 7

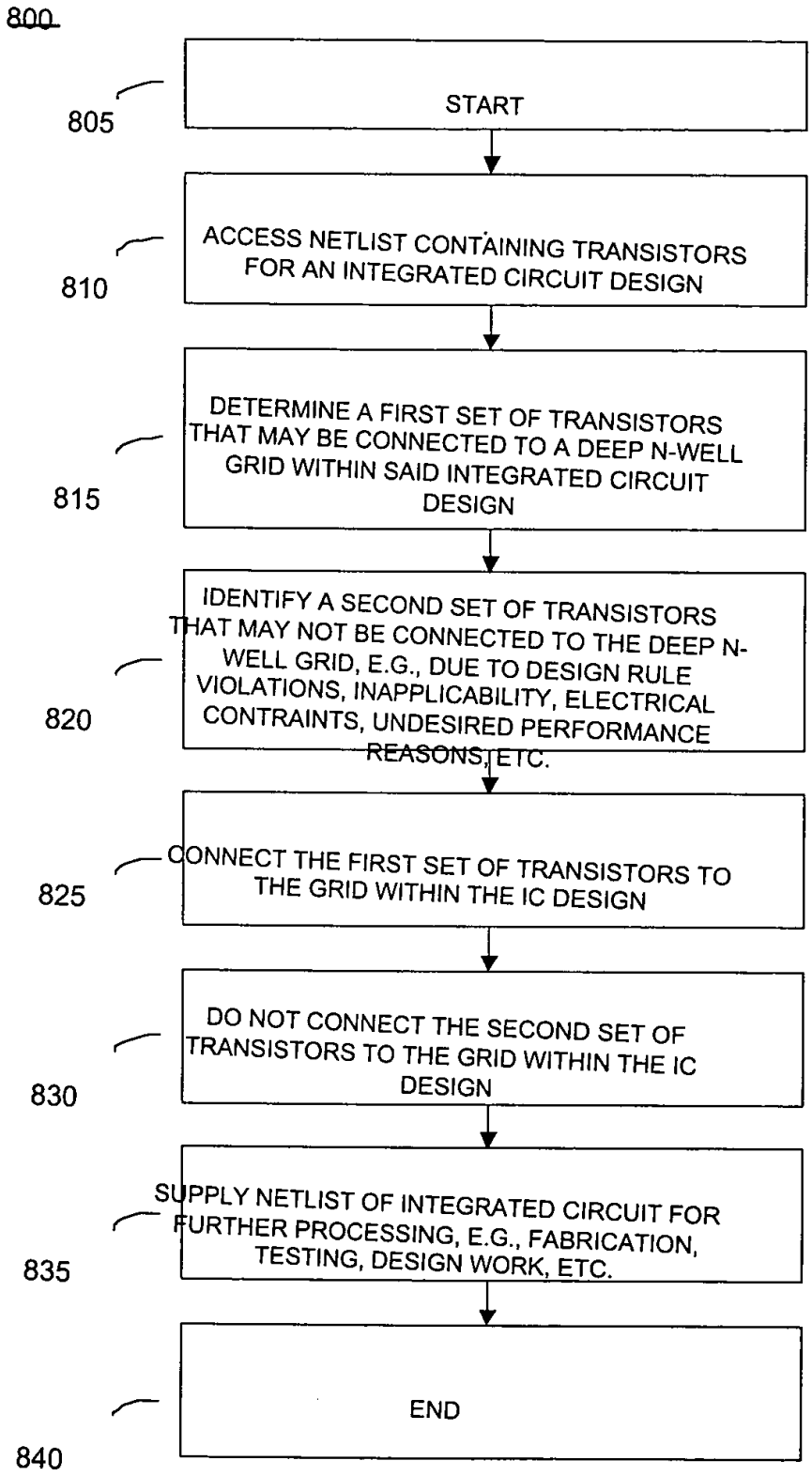
800
805
START
810
ACCESS NETLIST CONTAINING TRANSISTORS FOR AN INTEGRATED CIRCUIT DESIGN
815
DETERMINE A FIRST SET OF TRANSISTORS THAT MAY BE CONNECTED TO A DEEP N-WELL GRID WITHIN SAID INTEGRATED CIRCUIT DESIGN
820
IDENTIFY A SECOND SET OF TRANSISTORS THAT MAY NOT BE CONNECTED TO THE DEEP N-WELL GRID, E.G., DUE TO DESIGN RULE VIOLATIONS, INAPPLICABILITY, ELECTRICAL CONTRAINTS, UNDESIRED PERFORMANCE REASONS, ETC.
825
CONNECT THE FIRST SET OF TRANSISTORS TO THE GRID WITHIN THE IC DESIGN
830
DO NOT CONNECT THE SECOND SET OF TRANSISTORS TO THE GRID WITHIN THE IC DESIGN
835
SUPPLY NETLIST OF INTEGRATED CIRCUIT FOR FURTHER PROCESSING, E.G., FABRICATION, TESTING, DESIGN WORK, ETC.
840
END

Figure 8